

Claim Amendments

1 1. (canceled without prejudice) ~~An apparatus for adding a plurality~~
2 ~~of partial products comprising:~~

3 ~~a plurality of carry save adders coupled together in series, each of the~~
4 ~~carry save adders in the series receiving one of the plurality of partial products~~
5 ~~and two intermediate vectors from a prior carry save adder in the series of carry-~~
6 ~~save adders, and outputting a carry bit, a sum bit and two intermediate vectors,~~
7 ~~wherein the first one in the series of carry save adders receives two of the~~
8 ~~plurality of partial products;~~

9 ~~a last carry save adder coupled to a last one in the series of carry save~~
10 ~~adders and receiving a last partial product of the plurality of partial products and~~
11 ~~two intermediate vectors from a last one in the series of carry save adders, and~~
12 ~~outputting a carry vector (Cmsb) and a sum vector (Smsb);~~

13 ~~a plurality of carry propagate adders coupled in series and coupled to the~~
14 ~~plurality of carry save adders, each of said plurality of carry propagate adders~~
15 ~~outputting a resulting bit and a carry bit; and~~

16 ~~an output register coupled to the first one in the series of carry save~~
17 ~~adders, the last carry save adder, and the plurality of carry propagate adders, and~~
18 ~~storing the plurality of resulting bits, the sum bit output by the first one in the~~
19 ~~series of carry save adders and the carry bit output by the last one in the series of~~
20 ~~carry propagate adders.~~

1 2. (canceled without prejudice) ~~The apparatus according to claim 1,~~
2 ~~further comprising:~~

3 ~~a MOST SIGNIFICANT BIT carry output register coupled to the last~~
4 ~~carry save adder and storing the most significant bit carry vector (Cmsb); and~~

5 ~~a MOST SIGNIFICANT BIT sum output register coupled to the last~~
6 ~~carry save adder and storing the most significant bit sum vector (Smsb).~~

1 3. (canceled without prejudice) ~~The apparatus according to claim 1,~~
2 ~~wherein at least one of the carry-propagate adders comprises a half-adder and the~~
3 ~~other carry-propagate adders comprise full-adders.~~

1 4. (canceled without prejudice) ~~An apparatus for adding a plurality~~
2 ~~of partial products comprising:~~

3 ~~a plurality of carry-save adders coupled together in series, each of the~~
4 ~~plurality of carry-save adders receiving a successive one of the plurality of partial~~
5 ~~products and two intermediate vectors (In-1, In-2) from a prior carry-save adder~~
6 ~~in the series of carry-save adders and each of the plurality of carry-save adders~~
7 ~~outputting a carry bit (Cn-1) a sum bit (Sn-1) and two intermediate vectors (In,~~
8 ~~In+1) wherein a first one in the series of carry-save adders receives two of the~~
9 ~~plurality of partial products;~~

10 ~~a last carry-save adder coupled to a last one in the series of carry-save~~
11 ~~adders, receiving a last one of the plurality of partial products and two~~
12 ~~intermediate vectors from said last one in the series of carry-save adders, and~~
13 ~~outputting a plurality of sum bits and a plurality of carry bits; and~~

14 ~~a plurality of half-adder/full-adder series combinations coupled to the last~~
15 ~~carry-save adder, each of the plurality of half-adder/full-adder series combinations~~
16 ~~receiving two carry bits of the plurality of carry bits output by the last carry-save~~
17 ~~adder and two sum bits of the plurality of sum bits output by the last carry-save~~
18 ~~adder, and outputting two result bits and a carry bit.~~

1 5. (currently amended) ~~The apparatus according to claim 4, further~~
2 ~~comprising:~~

3 An apparatus for adding a plurality of partial products comprising:

4 a plurality of carry-save adders coupled together in series, each of the
5 plurality of carry-save adders receiving a successive one of the plurality of partial
6 products and two intermediate vectors (In-1, In-2) from a prior carry-save adder

7 in the series of carry-save adders and each of the plurality of carry-save adders
8 outputting a carry bit (C_{n-1}) a sum bit (S_{n-1}) and two intermediate vectors (I_n ,
9 I_{n+1}) wherein a first one in the series of carry-save adders receives two of the
10 plurality of partial products;

11 a last carry-save adder coupled to a last one in the series of carry-save
12 adders, receiving a last one of the plurality of partial products and two
13 intermediate vectors from said last one in the series of carry-save adders, and
14 outputting a plurality of sum bits and a plurality of carry bits;

15 a plurality of half-adder/full-adder series combinations coupled to the last
16 carry-save adder, each of the plurality of half-adder/full-adder series combinations
17 receiving two carry bits of the plurality of carry bits output by the last carry-save
18 adder and two sum bits of the plurality of sum bits output by the last carry-save
19 adder, and outputting two result bits and a carry bit;

20 two half-adders coupled together in series and coupled to the last carry-
21 save adder, said two half-adders receiving from the last carry-save adder two most
22 significant carry bits and a most significant sum bit and outputting two result bits
23 and a carry bit as a plurality of most significant bits of the result of adding the
24 plurality of partial products.

1 6. (previously amended) The apparatus according to claim 5, further
2 comprising

3 a single output register coupled to the plurality of half-adder/full-adder
4 combinations and storing the two result bits and the carry bit output by each of the
5 plurality of half-adder/full-adder series combinations.

1 7. (currently amended) A method of reducing the speed of a multiplier
2 comprising the step of:

3 replacing carry and save registers ~~[49a, 49b]~~ relating to a set of least significant
4 bits with a single register ~~[48]~~ and a carry-propagate adder comprising a half adder ~~[37]~~
5 and a set of full adders ~~[38-40]~~.